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A Stable Active Frequency Multiplier for RF/ Microwave Applications

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***Abstract*- The design & simulation of a stable VHF frequency multiplier for low power RF/microwave communication applications is presented. A novel technique has been used to stabilize the device & provide desired terminations to unwanted harmonics at both the output & input of the device, thereby ensuring stability to multiplier operation as well as providing sufficient rejection to the unwanted harmonics in the output signal.**

1. Introduction:

Frequency multipliers are basically non-linear circuits. All electronic circuits, for that matter, are non-linear, whether weakly or strongly non-linear. A perfectly linear circuit doesn't actually exist in practice. Whilst non-linearities are undesirable and degrade the performance of linear circuits such as small-signal amplifiers, circuits like multipliers utilize the non-linear behavior of their circuit elements to achieve frequency multiplication. In the absence of non-linearities, circuits like mixers, oscillators, multipliers would not exist.

This work focuses on the design of a single ended bipolar transistor frequency doubler in the VHF frequency band. The author wishes to emphasize that stability of the circuit is of utmost importance in its performance as instability can cause the circuit to malfunction and lead to total loss of functionality in the application where it is deployed. One can survive with slightly lower conversion gain, lower output power, average VSWR, even some exacerbation in spurious or noise floor levels, as this would mostly result in some degradation of performance. However, oscillations caused by an unstable device or circuit may lead to total loss of functionality, including damage to the device.

2. Design Details:

A. Multiplier Design Theory:

The design considers an active multiplier, using a bipolar device. It exhibits a Class-B multiplier with low input power. Bipolar devices have a strongly non-linear Base-Emitter capacitance characteristic. The device is biased near the turn on point so that the channel conducts current in pulses with duty cycle of ~50%. Device is terminated in short circuit at all undesired harmonics of input excitation, at both the input & output ports. Low power class B multipliers are most stable; and apart from having a good efficiency, gain & output power, they are also the most practical form of active frequency multipliers.

Fig.1 shows the circuit of an ideal bipolar frequency multiplier. When the input RF power to a device is low, i.e. small signal, the transistor operates in linear region. As the input power is increased, the gain of the device gets compressed as the transistor enters into the non-linear region. With the onset of non-linearity, the level of the harmonics begins to rise in the output, as the power gets divided between the fundamental and the harmonic components of the output spectrum.

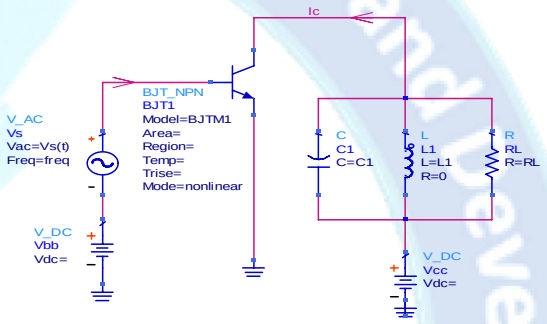

Fig.1. Ideal BJT Frequency Multiplier Circuit

For an n-th order multiplier, the output resonator circuit is tuned to the n-th harmonic of the excitation frequency. It thus effectively short circuits the collector at all other harmonics, especially the fundamental. The BJT's junction conducts only during the positive half cycle; hence the collector conducts in pulses. Collector current is composed of:

$$I_c(t) = I_0 + I_1 \cos(\omega_p t) + I_2 \cos(2\omega_p t) + I_3 \cos(3\omega_p t) + \ldots..$$

Since the tuned circuit in Fig. 1 is an open circuit at the desired harmonic frequency $n\omega_p$, all of the n-th harmonic current I_n circulates in the load R_L & hence contributes to the output power. The basic objective in the design of the multiplier is to ensure that the circuit remains unconditionally stable, and unwanted harmonics in both the input & output networks are properly terminated in short circuits. This shall ensure that no currents are circulating at the undesired frequencies in both the input & output of the device; thereby leading to not only obtaining the required power at the desired output frequency but also stable multiplier operation.

B. Device Model

Several BJT models have been presented till date, however due to its legacy and availability in most of the circuit simulators, the SPICE Gummel-Poon (SGP) model is widely used. The SGP model is the basic model which describes the main characteristics and features of a bipolar device operation.

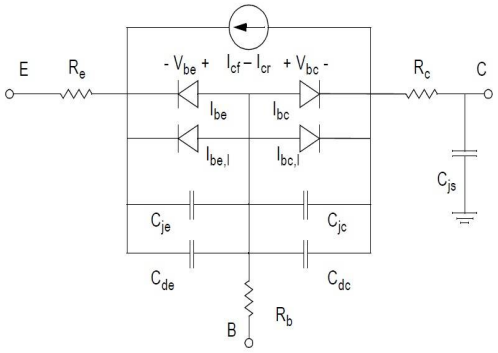

Fig.2. Non-linear BJT Equivalent Circuit Used in Gummel-Poon Model [4]

As shown in Fig. 2, large-signal equivalent circuit of a bipolar transistor includes various nonlinear elements such as contact resistances Re, Rc, and Rb, and parasitic collector-substrate capacitance, Cjs. Elements Cde and Cdc represent the diffusion capacitances, while Cje and Cjc represent the depletion components of the Base-Emitter and Base-Collector capacitances. The pair of diodes shown in the model, which are marked with the currents Ibe,l and Ibc,l, model Base-Emitter and Base-Collector leakage. [4]

C. Multiplier Operation

Bipolar devices have a large, strongly non-linear Base-Emitter capacitance characteristic which is responsible for the non-linear behavior of the bipolar device. This inherent B-E capacitance is exploited for generating the harmonics. By changing the conduction angle of the transistor, required harmonics can be enhanced while the unwanted ones can be reduced. Suitable filtering is however necessary at the collector to select the desired harmonic and reject the unwanted ones with minimal loss of power. Also, due to the B-E capacitance, BJTs are susceptible to oscillations, which can be avoided by short-circuiting the base & collector at all unwanted frequencies.

The bipolar transistor used in the design is biased at the required V_{CE} and I_C using the DC bias network. As long as the excitation signal power is low, the output signal is perfect sinusoidal and the device exhibits linear behavior. However, as the input power is increased, it results in increase in the voltage swing at the input. Correspondingly, the output voltage cycle gets truncated, leading to onset of non-linearity and generation of harmonics in the output circuit.

D. Design Objective

The objectives of the design are listed out in Table 1.

Table 1: Performance Objectives

Sl. No.	Parameter	Specification
1.	Input Frequency	120 MHz
2.	Output Frequency	240 MHz
3.	Conversion Gain @ Pin = -2 dBm	2 dB (min)
4.	Harmonics Level	< 15 dBc
5.	Return Loss	< 10 dB

E. Design Approach

The basic block schematic of the multiplier circuit is shown in Fig.3.The design process began with the selection of a suitable device, in this case a bipolar transistor, which is basic non-linear element in the multiplier circuit. Choosing a suitable base medium or substrate for realization of the design was the next obvious step. All these choices were largely dictated by the frequency & power requirements of the design, and of course, the availability. This was followed by finalizing the multiplier circuit topology and the DC bias level. Device stabilization and RF design, including the design of idler circuits and matching networks for the source & load impedance matching, followed by circuit optimization for achieving the performance objectives were the final steps in the design.

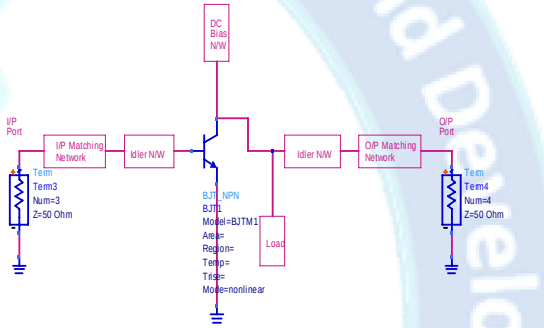

Fig.3. Frequency Multiplier Block Schematic

Fig.3 depicts the basic multiplier circuit block schematic. At design level, instability in the circuit leads to failure of non-linear analysis due to lack of convergence in simulation tools. Design process included choosing the proper device, substrate and the circuit topology. Based on the frequency of operation and performance objectives, it was decided to use Agilent's general purpose medium power BJT AT-42070. The circuit was decided to be designed in planar microstrip configuration since microstrip lines have a rugged structure, and can handle sufficiently high voltages & currents. Also, its top surface is easily accessible, so surface mount components & devices can be easily mounted; it also provides the flexibility of minor post-fabrication variations & tuning. Both the RF & DC signals can also be easily transmitted. A single ended active multiplier topology was thereby selected.

3. RF Design:

A. DC Biasing

Datasheet of the selected device AT-42070 was examined for selecting the biasing conditions. Multiplier operates as a Class-B amplifier with low input power. The device is biased near the turn on point so that the channel conducts current in pulses with duty cycle of ~50%.

Transistor is biased in CE configuration with fixed bias as shown in the Fig. 4. The value of the biasing resistors was chosen to provide an operating point with V_{CE} = 6 Volts, I_c = 8 mA

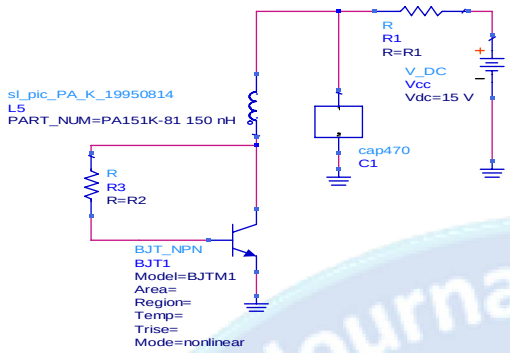

Fig.4. Transistor Biasing Circuit

B. Device Stabilization

Unconditional stability and sufficient rejection of the harmonics was the corner stone of the author's multiplier design. The issue of stability & the technique used to achieve it over the operating frequency range is dealt with first.

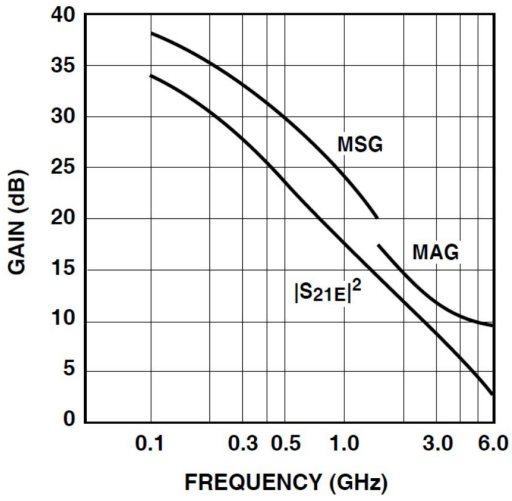

Fig.5. Power Gain, MSG & MAG of AT-42070 vs Frequency @ T_A=25^{0}C

A quick look at the device datasheet, as shown in Fig. 5 reveals that the device has a maximum stable gain (MSG) of ~37 dB at the excitation frequency of 120 MHz. Such high gain renders the device susceptible to oscillations, unless stabilized.

One approach towards achieving stability could have been to make the multiplier circuit stable rather than making the device stable. In such a case the device, and hence the multiplier, could have yielded higher conversion gain as well as output power. However, this approach carried the risk of instability as the device in such a case would have been only conditionally stable. Hence, any variations in operating conditions, including the voltage, current, terminating port impedances, temperature, etc. would have rendered the circuit vulnerable to oscillations and instabilities, which was not acceptable as per the design specifications & application.

Author therefore chose the other approach of making the transistor itself as unconditionally stable first, and then proceeding with the remaining part of multiplier design. Although this meant sacrificing the conversion gain and output power significantly, it did ensure easier convergence of non-linear simulation as well as stable multiplier functioning under any condition.

Hence, in order to stabilize the device and to make it unconditionally stable, gain was reduced by loading the device both at the input (base) and output (collector), as follows:

a. a. Series Resistive Loading at the Input (Base)

A Series resistance (5-10 ohms) was introduced at the input to reduce the gain and stabilize the device.

b. Shunt Resistive Loading at the Output (Collector)

Collector of the transistor was loaded with a suitable resistance (200-250 ohms) to stabilize the device. A high value capacitance was also added in series with the loading resistor, not only to act as a DC block (to isolate it from collector DC bias) but also to ensure uniform wideband RF loading to the transistor. Specifically, a self designed model of the capacitor, developed from the manufacturer's data of the self resonant frequency response of the capacitor, was used in simulation. This was crucial in ensuring wideband uniform loading & thereby a stable multiplier operation.

Upon simulation, it was observed that with the proper value of the loading elements, the gain of the device was sufficiently reduced and the device became unconditionally stable at the operating input & output frequencies. However, it had its own effect on reducing the conversion gain as well as the output power. But since multiplier stability was the foremost criteria in the circuit design, it was unavoidable. However, due to the available margins, and by carefully choosing values of the loading elements, optimum loading could be achieved which ensured unconditional stability of the device, and acceptable power gain & available output power of the transistor.

C. Harmonics Termination

Providing suitable termination to the harmonics was the other most important criteria in the design on the following three counts:

a. Rejection of Harmonics: Design performance specifications of the multiplier require the level of harmonics to be below 15 dBc at the output. A doubler means that the fundamental and all other harmonics except second should be well below the second harmonic at the output of the multiplier.

b. Stability: As explained earlier, if the undesired harmonics are not terminated in short circuits, then currents at these frequencies keep circulating in the input & output networks. This not only causes loss of power, but also leads to instability.

c. Convergence in HBA: As indicated later, non-linear simulation does not converge to a solution if the undesired harmonics are not terminated properly or the circuit is unstable.

Hence, it was evident that providing suitable termination to the harmonics was one of the most crucial steps in the design. In order to achieve this, following strategy was adopted:

a. Providing short circuit to the 2nd harmonic at the input of the device. This was required because this being a doubler circuit, the 2nd harmonic was desirable at output, but not at input. Presence of 2nd harmonic current circulating in the input circuit would have made the circuit unstable and also lead to failure of convergence in HBA simulation.

b. Due to the input and output frequencies falling in the VHF band, it was decided to employ series resonant LC circuits or Idlers, resonant at the required frequency, using a combination of lumped and distributed components, to present a short circuit to the required harmonics, both at input and output..

Achieving a precise resonant frequency of these idler circuits was a key component in ensuring a robust and stable design of the multiplier circuit. In order to ensure this, the following steps were taken:

i. Instead of using ideal components, which would have ignored the high frequency effects, all the lumped components were replaced by their high frequency equivalent models. These models incorporated the effect of all the parasitic capacitances and lead inductances in the components. Some of the models were provided by their manufacturers in the elements library of the ADS simulator. This ensured that the performance of the idler would remain unchanged when the circuit gets fabricated & used in the intended application.

ii. It was important to ensure that the device sees a perfect short looking in the direction of the idler circuit, at that particular frequency. In order to achieve this, the series resonant frequency of the circuit should be exactly same as the harmonic frequency. Hence, during simulation, each idler was designed separately with the actual circuit layout of the PCB, modeling each and every discontinuity like bends, steps, gaps etc. properly.

iii. The entire electrical length of the transmission line, from the tip of the transistor lead (base or collector) to the grounding point of the idler circuit was modeled and considered during simulation. As is known, for achieving a perfect short circuit, following condition needed to be satisfied:

Reflection Coefficient, $\Gamma in = 1 \angle 180^0$

Simulation was carried out, and value of L and C was optimized carefully in each idler circuit to obtain the magnitude and angle of the Reflection Coefficient, at the device lead, precisely equal to 1 and 180^0 respectively at the harmonic frequency. This was the single most crucial step in order to provide the suitable termination to unwanted harmonics, thus achieving a stable frequency multiplier performance.

D. Matching Network Design

After stabilizing the device, and providing the suitable termination to all unwanted harmonics, the next part was to design suitable input and output matching networks, to match the multiplier circuit with the input and output impedances. Design of the matching circuit and its optimization for rated performance, viz. the conversion gain, output power, and input/ output VSWR were the final important steps in the design.

First cut design of the matching networks was obtained from large signal S-parameters of the composite circuit consisting of the device with loading and idler circuits. Lumped components were used as the input frequency was 120 MHz and the output frequency was 240 MHz. As before, high frequency models of the lumped components, obtained from the elements library were used to obtain accurate frequency response of the circuit.

This part of the design was carried out using Non-linear simulation, or the HBA simulator of ADS.

4. Harmonic Balance Analysis

In Harmonic Balance Analysis, all linear reactances, impedances, transmission lines are lumped into a single matrix. The linear part of the circuit can be treated as a multiport, and it needs to be evaluated only once at each harmonic, with the results stored as matrices. The circuit can then be partitioned into a linear sub-circuit and non-linear sub-circuit.

The linear sub-circuit can be described by S-parameters or Y-parameters, while the non-linear sub-circuit are modeled by their I/V or Q/V characteristic and analysed in time domain. The circuit is then reduced to an N+2 port network with non-linear elements connected to N-ports, and input & output at N+1 and N+2 port respectively. The source and load impedances are absorbed in the linear sub-circuit.

The circuit is successfully analyzed when either the steady state voltage or current waveforms at all ports is known, or the frequency components at all ports is known. The idea of HBA is to find a set of voltage waveforms (or alternatively the harmonic voltage components) at each port that gives the same currents in both the linear & non-linear network equations. When that set is found, it is a solution.

The HBA simulator works as follows:

i. It basically divides the circuit into linear & non-linear sub-circuits.
ii. It starts by making an initial estimate of the voltage at all harmonics at each node.
iii. Linear sub-circuit is analyzed in Frequency Domain to obtain linear circuit currents.
iv. Currents in the non-linear sub-circuit are obtained by analyzing in Time Domain using device I/V characteristic. It is then converted into frequency domain using Fourier analysis.
v. Hence, currents flowing away from each node are available at all frequencies. By applying KCL at each node & at each frequency, algebraic sum of all currents should be zero (or some error value).

vi. If KCL is not satisfied, then initial estimate of node voltages is changed iteratively to reduce error to zero or some pre-defined small value.
vii. Same steps are repeated for another power & frequency.
viii. Hence, set of harmonic currents at each node is obtained. Thus power level in each harmonic is ascertained.

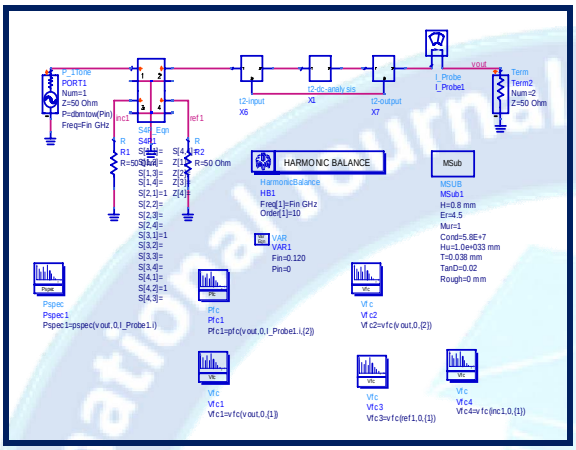

Fig.6. Harmonic Balance Analysis Test Bench

Basic inputs to the simulator include the excitation frequency, input power and the no. of harmonics for which the simulator would make the calculations. After the initial bias setting, and loading the device for stabilizing, idler circuits consisting of resonant networks at unwanted harmonics were placed in shunt at both the input & output of the device.

The next step in the design was conjugate matching of circuit input impedance to the source, and the output to the load. Based on an initial estimate of the matching network elements using the large signal analysis, the circuit was carefully analyzed using HBA simulation. Test bench for the HBA simulation is shown in Fig. 6.

The analysis was started with an initial value of low input power and less number of harmonics to achieve faster convergence. Since the circuit was already stabilized, solution convergence was expected to be achieved easily. With minor tweaking of the circuit elements, a rough performance of the circuit was achieved initially. Slowly, and iteratively, the number of harmonics was raised up to 10, to get better accuracy in result. However, this also led to several instances of failures in convergence. Iteratively, the input power was also raised slowly, step by step, to achieve the required output power and conversion gain. Multiplier circuit was optimized to meet all the performance specifications as shown in the next section.

5. **Simulation Results:**

Harmonic balance analysis of the multiplier yields the output power in the desired as well as undesired harmonics, and input/ output return losses. The circuit is optimized for maximum conversion gain, return losses & rejection of harmonics, with unconditional stability. Multiplier simulation results showing output power, conversion gain, harmonic levels and return loss for various input power levels is shown in Table II. The doubler achieves a **conversion gain of 3.1 dB at Pin = -2 dBm**, with return loss better than 20 dB.

Table 2.: Multiplier Simulated Performance

freq	...(HB.Pspec1)+30	IRL	Pin	...log(HB.Pfc1)+30
Pin=-3.000			-3.000	0.459
0.0000 Hz	<invalid>	<invalid>	-2.000	1.112
120.0MHz	-30.541	-24.977 / -3.694	-1.000	1.682
240.0MHz	0.459	<invalid>	0.000	2.181
360.0MHz	-63.403	<invalid>	1.000	2.622
480.0MHz	-69.415	<invalid>		
600.0MHz	-70.417	<invalid>		
720.0MHz	-66.178	<invalid>		
840.0MHz	-64.682	<invalid>		
960.0MHz	-65.111	<invalid>		
1.080GHz	-62.264	<invalid>		
1.200GHz	-65.548	<invalid>		
Pin=-2.000				
0.0000 Hz	<invalid>	<invalid>		
120.0MHz	-30.391	-25.100 / -3.542		
240.0MHz	1.112	<invalid>		
360.0MHz	-61.889	<invalid>		
480.0MHz	-67.994	<invalid>		
600.0MHz	-68.788	<invalid>		
720.0MHz	-63.955	<invalid>		
840.0MHz	-62.637	<invalid>		
960.0MHz	-62.521	<invalid>		
1.080GHz	-59.659	<invalid>		
1.200GHz	-62.452	<invalid>		
Pin=-1.000				
0.0000 Hz	<invalid>	<invalid>		
120.0MHz	-30.265	-25.219 / -3.424		
240.0MHz	1.682	<invalid>		
360.0MHz	-60.534	<invalid>		
480.0MHz	-66.459	<invalid>		
600.0MHz	-67.518	<invalid>		
720.0MHz	-61.805	<invalid>	Eqn IRL=(HB.ref1/HB.inc1)*(HB.ref1/HB.inc1)	
840.0MHz	-60.910	<invalid>		
960.0MHz	-60.162	<invalid>		
1.080GHz	-57.449	<invalid>		
1.200GHz	-59.714	<invalid>		
Pin=0.000				
0.0000 Hz	<invalid>	<invalid>		
120.0MHz	-30.155	-25.335 / -3.345		
240.0MHz	2.181	<invalid>		
360.0MHz	-59.326	<invalid>		
480.0MHz	-64.817	<invalid>		
600.0MHz	-66.565	<invalid>		
720.0MHz	-59.819	<invalid>		
840.0MHz	-59.338	<invalid>		
960.0MHz	-58.063	<invalid>		
1.080GHz	-55.384	<invalid>		
1.200GHz	-57.170	<invalid>		
Pin=1.000				
0.0000 Hz	<invalid>	<invalid>		
120.0MHz	-30.057	-25.449 / -3.311		
240.0MHz	2.622	<invalid>		
360.0MHz	-58.251	<invalid>		
480.0MHz	-63.129	<invalid>		
600.0MHz	-65.853	<invalid>		
720.0MHz	-58.090	<invalid>		
840.0MHz	-57.760	<invalid>		
960.0MHz	-56.270	<invalid>		
1.080GHz	-53.365	<invalid>		
1.200GHz	-54.912	<invalid>		

As can be seen from the output spectrum plot, the multiplier has comfortably achieved sufficient rejection of unwanted harmonics. Table II and Fig.7 clearly show that the level of all the harmonics is at least 30 dB below the output carrier.

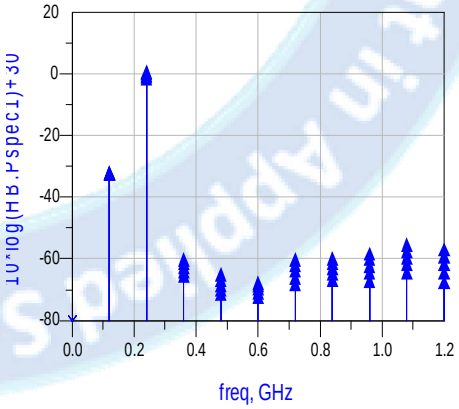

Fig.7. Output Spectrum at various power levels

Non-linear simulation converges easily to a solution over the entire range of input power levels, as indicated in the simulation results. Also, very little change in performance was observed over minor variations in values of circuit elements

and operating conditions. This clearly indicates that the doubler circuit has achieved the stability requirement of the design comfortably.

6. Scalability & Future Scope:

The multiplier design presented can be appropriately scaled for higher order multiplication as well as higher or lower frequencies. The design approach for such a scaled up version would be the same. However, as can be easily predicted, the choice of substrate, device and components shall be dictated by the frequency of operation and the multiplication factor, as well as output power and available input power. Accordingly, various active devices like MESFETs, HEMTs, HBTs etc. and passive devices like SRD and Varactors can be considered.

The choice of substrate, active device, components, PCB layouting etc was done carefully, making sure that Hi-Rel version of each of these design elements is available, if required. This has ensured that the same design can be qualified, without any change, if required for use in hi-rel applications. It would only require using MIL grade screening, qualified processes and quality control to convert this to Frequency Doubler circuit fit for deployment in such applications, if required.

7. Conclusion:

As the presented simulated results and the achieved performance with adequate margins show, all design goals have been met comfortably. Adequate care was taken during each stage of design to simulate all the deterministic variables and tolerances, including components, grounding, DC bias, parasitics associated with components, wires, ribbons etc. Special attention was also focused on modeling all the discontinuities, whether in the circuit layout, RF launch points. Crucial aspect of grounding was also given due weightage and the complete electrical length from the node to the grounding point was properly modeled and considered in simulation. This gives the confidence that the simulated performance of the circuit would be a close replica of the actual circuit performance.

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