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VHDL Implementation of 32- bit Dual way Switching System with caller ID Facility using Opcode

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Abstract: In this paper we work on Landline Switching for two different channels using VHDL each channel have 16 users. They can communicate either intra channel or inter channel. We are also providing Caller ID facility in our work. In this work, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively. We are using 32 bit Opcode for communication between these channels or with in the channel. In this work we can define all the functions by Opcode. Opcode is responsible for caller id also and which data we are going to transmit or receive. We implement our work by Xilinx ISE i.e. responsible for synthesis also. For simulation we are using Modelsim 10.2a.

Keyword: Data Transmission, Opcode, VHDL, Switching.

1. Introduction:

In present scenario of the technology, there are two fields in engineering that hold great demand in the industry; communication and VLSI. The people want to connect themselves to anyone, anytime and anywhere. We have already experienced a huge development from a simple morse code telegram to the highly sophisticated triple play broadband ISDN, or nonetheless the Satellite Communication. This might give you ways to communicate with speech, that's no big deal; in fact the amazing part starts when real time audio, video and data can be integrated for communication. But at present there is also a second stringent demand that is miniaturization. The race is on for reaching the minimum space as much as possibly occupied by the systems. This paper, keeping an eye wide open on the future, has mixed both fields enabling us to communicate, in a digital manner, by using systems that would be integrated on an IC through programming of the IC using VHDL.

VHDL is a language for describing digital electronic systems. There was a need for a standard language for describing the structure and function of integrated circuits (ICs). Hence the VHDL was developed, and subsequently adopted as a standard by the Institute of Electrical and Electronic Engineers (IEEE) in the US. VHDL is designed to fill a number of needs in the design process. Firstly, it allows description of the structure of a design that is how it is decomposed into sub-designs, and how those sub-designs are interconnected. Secondly, it allows the specification of the function of designs using familiar programming language forms. Thirdly, as a result, it allows a design to be simulated before being manufactured, so that designers can quickly compare alternatives and test for correctness without the delay and expense of hardware prototyping [1].

This work focuses more on the programming part rather than the hardware. We have explained every model in detail with their opcodes (user defined), underlying architecture and programming. Along with that the simulation results are also provided, showing transfer of data from input subscriber to output subscriber using sequential write/ random read method with timing information. To verify the transfer of data from input subscriber to the output subscriber a 16 bit op-code is assumed in which each bit represents a specific function.

2. Related Work:

Rajeev Sivaram et al, proposed as an attractive mechanism for efficiently implementing multicast and other collective operations on direct networks. However, applied this mechanism to switch-based parallel systems is nontrivial. In this work, they proposed alternative switch architectures with differing buffer organizations to implement multidestination worms on switch-based parallel systems. First, they discuss issues related to such implementation (deadlock-freedom, replication mechanisms, header encoding, and routing). Next, they demonstrate how an existing central-buffer-based switch architecture supporting unicast message passing can be enhanced to accommodate multidestination message passing. Similarly, implementing multidestination worms on an input -buffer-based switch architecture is discussed, and two architectural alternatives are presented that reduce the wiring complexity in a practical switch implementation. The central-buffer-based

and input-buffer-based implementations are evaluated against each other, as well as against the corresponding software-based schemes. Simulation experiments under a range of traffic (multiple multicast, bimodal, varying degree of multicast, and message length) and system size are used for evaluation. The study demonstrates the superiority of the central-buffer-based switch architecture. It also indicates that under bimodal traffic the central buffer- based hardware multicast implementation affects background unicast traffic less adversely compared to a software-based multicast implementation. These results show that multi destination message passing can be applied easily and effectively to switchbased parallel systems to deliver good multicast and collective communication performance. [10].

Krishna V. et al, main focus in that work establishes the energy savings derived by using probabilistic AND as well as NOT gates constructed from an idealized switch that produces a probabilistic bit (PBIT). A probabilistic switch produces the desired value as an output that is 0 or 1 with probability p, represented as a PBIT, and, hence, can produce the wrong output value with a probability. In contrast with a probabilistic switch, a conventional deterministic switch produces a BIT whose value is always correct. Our switch-based gate constructions are a particular case of a systematic methodology developed here for building energy-aware networks for computing, using PBITs. Interesting examples of such networks include AND, OR, and NOT gates (or, as functions, Boolean conjunction, disjunction, and negation, respectively). To quantify the energy savings, novel measures of "technology independent" energy complexity are also introduced here—these measures parallel conventional machine-independent notions of computational complexity such as the algorithm's running time and space. Networks of switches can be related to Turing machines and to Boolean circuits, both of which are widely known and well-understood models of computation. Our gate and network constructions lend substance to the following thesis (established for the first time by this author :The mathematical technique referred to as randomization yielding probabilistic algorithms results in energy savings through a physical interpretation based on statistical thermodynamics and, hence, can serve as a basis for energy-aware computing. While the estimates of the energy saved through PBIT-based probabilistic computing switches and networks developed here rely on the constructs and thermodynamic models due to Boltzmann, Gibbs, and Planck, this work has also led to the innovation of probabilistic CMOS-based devices and computing frameworks. Thus, for completeness, the relationship between the physical models on which this work is based and the electrical domain of CMOS-based switching will be discussed [11].

Ahmed F. Aref et al , proposed a fully integrated adaptive multiband multimode switching-mode power amplifier (SMPA) in CMOS technology. The power amplifier (PA) module, consisting of input matching, driver, output stage, load transformation network (LTN), and auxiliary circuitry, utilizes optimized driving waveforms to increase output power and efficiency of a SWPA. The PA module is packaged in a 32 quad flat no-lead package. Based on the detailed analysis on appropriate driving waveforms, the SMPA is designed to maximize its output power and efficiency with minimum on-chip harmonic terminations. Furthermore, an adaptive gain control technique is proposed to control the SMPA gain at back-off while boosting the power-added efficiency (PAE) using a fully integrated tunable LTN. Employing both techniques concurrently enables us to have a multiband multimode SMPA. Measurements on a PA module designed in 90-nm CMOS and incorporating theses findings result in peak PAE of 43% for an output power of 27.1 dBm, associated with a large-signal gain of 22.1 dB at 1.97 GHz, when the devices are biased at 2.8 V.With the tunable LTN PAE at 4- and 6-dB backoff is 30% and 23%, respectively. To our knowledge, this is the first fully integrated multiband multimode SMPA in CMOS technology. [12]

Dapeng Tian et al, worked on a switching-channel bilateral control with energy monitor (EM) was newly proposed to realize haptic communication through a wireless network. The varying delay in the communication line and the situation of duplex operation are considered. In such a system, human operators on two sides of the master–slave robots system feel the hardness of the remote environment placed on the contralateral side. The EM approach is presented to judge the role of the robot (manipulated by an operator or contacting an environment), which provides a beacon for the switching algorithm. The position tracking of the system is improved by switching off the channel of force control in the human manipulated robot. The problem of position drift in traditional methods is overcome. Disturbance observer is applied to simplify the design of the bilateral control law, and to guarantee the efficient force switching. Because of improved position tracking and satisfactory force fidelity, the proposed approach achieves more vivid haptic transmission. By experiments, the validity is verified. [13].

Prashant Rai et al, proposed a switching system implies data transmission between two communicating entities. This transmission can be either via trunks or it can be completely wireless, technically termed as Telephone Switching and Mobile switching, respectively. They report the implementation of a switching system using very high speed integrated circuit hardware description language (VHDL) which is more reliable and efficient than the present switching system. It converts entire bulky switching unit

which consists of routers, multiplexers, decoders, counters in to a single integrated circuit (IC). Simulation results was presented for transfer of data from input subscriber to the output subscriber using sequential write /random read mode with the timing diagram. To verify the transfer of data from input subscriber to the output subscriber a 16 bit op-code is assumed in which each bit represents a specific function. [14].

3. Methodology:

A major component of a switching system or an exchange is the input and output circuits called inlets and outlets. The primary function of the switching system is to establish a path between inlet and outlet. The hardware used is the switching network. If there are N inlets and M, outlets, when N=M the network is called symmetrical network. The inlets and outlets may be connected may be connected to local subscriber or trunk from / to other exchanges .when all inlets and outlets are connected to subscriber lines the logical connection appears, In this case the output lines are folded back to input and hence called the folded network.

Four types of connection can be established:

1. Local call connection between two subscribers in the system
2. Outgoing call connection between an incoming trunk and a local subscriber
3. Incoming call connection between an incoming trunk and a local subscriber
4. Transit call connection between an incoming trunk and outgoing trunk

Principle of Landline Switching

In this design, the data coming in through the inlets are written into the data memory and later read out to the appropriate outlets. The incoming and out coming data is usually in serial form whereas the data are written into and read out of the memory in parallel form. It therefore becomes necessary to perform serial to parallel conversion and parallel to serial conversion at the inlets and outlets respectively.

For convenience, the in and data out parts of the MDR are shown separately for the data memory. Since there is only one MDR a gating mechanism is necessary to connect the required inlet/outlet to MDR. This is done by the in gate and out gate units. The information is not transferred in real time: it is first stored in the memory and later transferred to the outlet. There is a time delay between the acquisition of a sample from an inlet and its delivery to the corresponding outlet. This switching system can be controlled in following three ways:

1. Sequential write/Random read.
2. Random write/Sequential read.
3. Random input/Random output.

In the first two methods of control, the sequential / random read / write operations refer to the read / write operations associated with the data memory. In both these cases, the inlets and outlets are scanned sequentially. In the last case, the inlets and outlets are scanned randomly, and the data memory is accessed sequentially.

Sequential write / random read:

In this method the inlets are scanned in the first phase one after another and the data is stored in the data memory sequentially. There is a one to one correspondence between the inlets and the locations of the data memory. The control memory locations contain the addresses of the inlets corresponding to the outlets.

Features:

- Dual way 32 user support
- Sequential Input Random Read
- Caller Id Facility
- Inter and Intra exchange
- 16 Bit data transfer
- Inband Signalling
- Synchronization clock
- Reset features

The opcode assumed is of 32 bit in which each bit is having some specific function. Starting from right hand side, the bit 0 to 15 represents data, bit 16-21 are zero, bit 22-25 represent source subscriber, bit 26-29 represent destination subscriber, bit 30 represent whether the call is interexchange or interexchange and bit 31 represent whether the subscriber is enabled or disabled.

E	I	D3	D2	D1	D0	S3	S2	S1	S0	X	X	X	X	X	X
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Fig 1: 32 bit OPCODE

Inter Exchange:

For inter exchange value of I will be 1 in that case 16 users in each exchange can communicate with each other. Exchange 1 have 16 user and Exchange 2 have 16 user if we are working on Inter exchange then 16 user of exchange 1 can communicate with 16 users of exchange 2 and also 16 user of exchange 2 can communicate with 16 users of exchange 1.

Intra Exchange:

For intra exchange value of I will be 0 in that case 16 users in one exchange can communicate with each other. Exchange 1 have 16 user and Exchange 2 have 16 user if we are working on Intra exchange then 16 user of exchange 1 can communicate with 16 users of exchange 1 only they cannot communicate with exchange 2 users and also 16 user of exchange 2 can communicate with 16 users of exchange 2 only they can not communicate with exchange 1 users.

Data Memory:
We have 17 bit of std_logic type data memory for 16 locations i.e. we can have 16 bit of data which we can transfer for intra exchange exchange1 to exchange1 all users and exchange 2 to exchange 2 all users. In case of Inter Exchange we can transfer 16 bit of data exchange 1 to exchange 2 all 16 users and exchange 2 to exchange 1 all 16 users.

Control Memory:
We have 16 locations of integer type for control memory. It decide all the function of whole system i.e. which exchange of caller want to communicate which exchange user. It will decide by caller id of all users and they have what data all information is passing through control memory.

Caller ID:
We have 32 location 16 locations for source and 16 locations for destination. If exchange1 work as a source for intra exchange then destination will be exchange1 in this case Caller ID will decide that which location will receive the data and also tell to destination that which location transmit this data. If exchange1 work as a source for inter exchange then destination will be exchange2 in this case Caller ID will decide that which location will receive the data and also tell to destination that which location transmit this data. If exchange2 work as a source for intra exchange then destination will be exchange2 in this case Caller ID will decide that which location will receive the data and also tell to destination that which location transmit this data. If exchange2 work as a source for inter exchange then destination will be exchange1 in this case Caller ID will decide that which location will receive the data and also tell to destination that which location transmit this data.

Working Specifications:
Phase 1: Input Subscribers in both the exchanges are scanned sequentially. It takes 16 clock cycles to scan 32 subscribers in order to know their status, that is they want to transmit or not. This is called a sequential scanning. The date to be transmitted is stored in data memory in sequential order. The information relating to the called subscriber is stored in control memory in sequential order and caller id number is stored in the caller id memory in the sale way. Thus we can say system is sequential write.

Phase 2: When all the scanning is finished the location of the data memory is read according to the corresponding location of the control memory. For example, if first location of data memory has data 'd' and corresponding location in control memory is 2, this means that 'd' will be communicated to the 2nd user of the exchange, thus we can say the system is random read.

To decide where the data will be communicated we use a bit in our op code as 'I' bit. If 'I' =1, then it is interexchange, i.e. the read out data will be given to user of other exchange. Thus communication between the subscriber of two exchanges can be made possible and hence the name interexchange.

If 'I' = 0, then it is called as intraexchange, i.e. the read out data, will be given to the user of the same exchange. Thus communication between subscribers of the same exchange is made possible, and hence the name Intraexchange.

The exchange between caller id memories is done only if the particular user is enabled. Same is the case with data memory. A particular user is enabled if its opcode 16th bit is 1 and disabled if it is 0.So caller must be enabled and called must be disabled in order to make a call successful. The communication means just to transfer the data (0- 15 bits of opcode) between entities and is shown by overwriting the data bits if called sub=scriber. Caller id facility enables the called user to see who is calling by checking his relevant bits of opcode (25 to 22) fig 3.2 shows the structure of switching system.

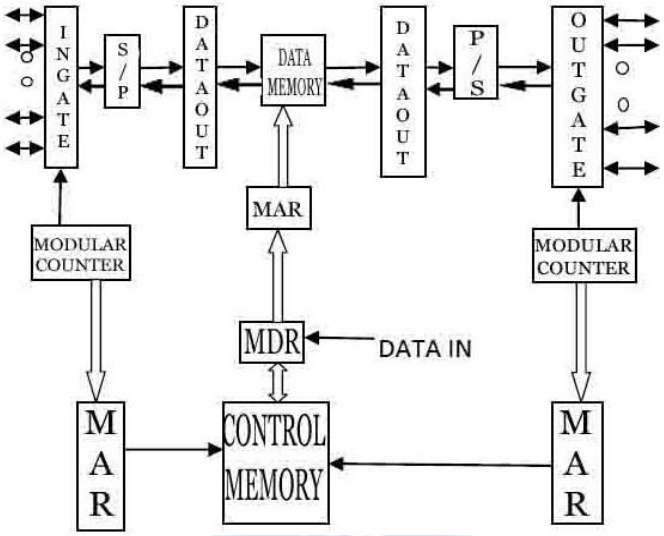

Fig 2: Dual Way Structure of Switching System

4. Result and Discussion:
There are two exchange centers which taken as 'din' and 'dout'. Our work has been implemented for inter exchange and Intra exchange both. If we take 'I' is one then our design will work for inter exchange. If we take 'I' is zero then our design will work for Intra exchange. Our design is depend on some more inputs clock, reset and enable. If reset is high then our design will not perform any function, all functions performed on low reset and positive edge of clock.

If enable is zero then there is no exchange of data. Our exchanges are work on high enable bit.
In this case we shows the inter exchange for first exchange. Here we take enable bit 1, I as 1, source address is 0101, destination address is 0110 data for transmission is "AD01". We receive that data on second exchange dout on 6th address shown in fig 3.

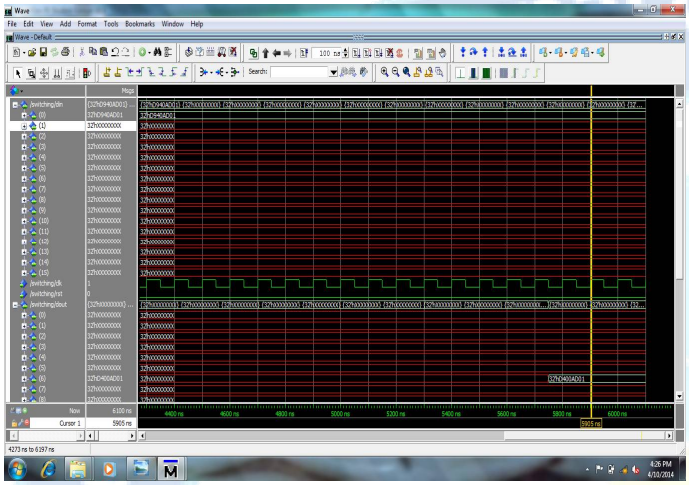

Fig 3: Simulation result for First Exchange (Inter Communication)

In this case we shows the intra exchange for first exchange. Here we take enable bit 1, I as 0, source address is 0110, and destination address is 0101 data for transmission is "AD01". We receive that data on first exchange din on 6th address shown in fig 4.

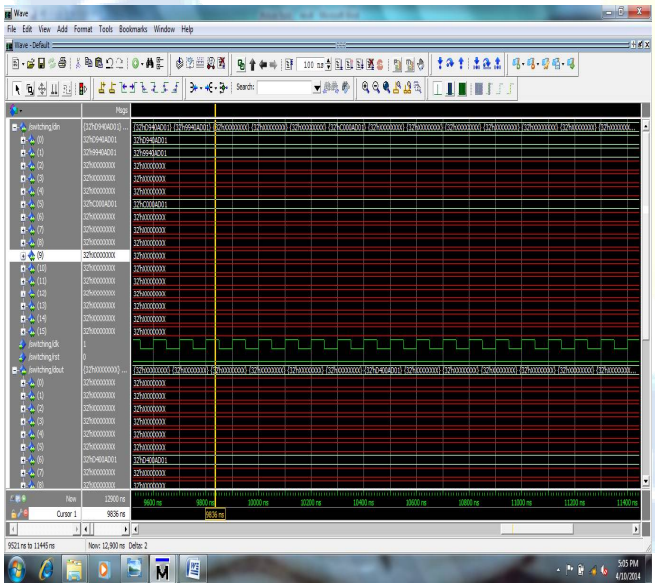

Fig 4: Simulation result for First Exchange (Intra Communication)

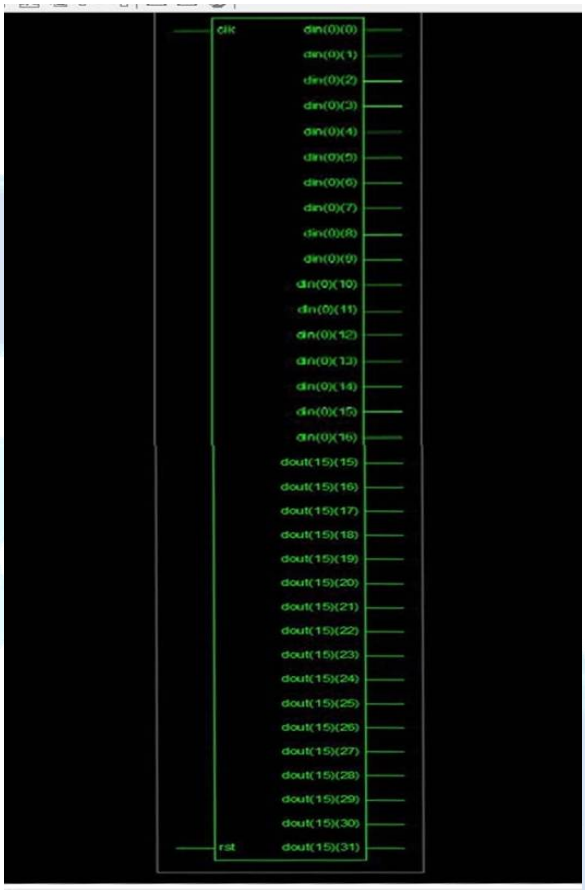

Fig 5: Main RTL

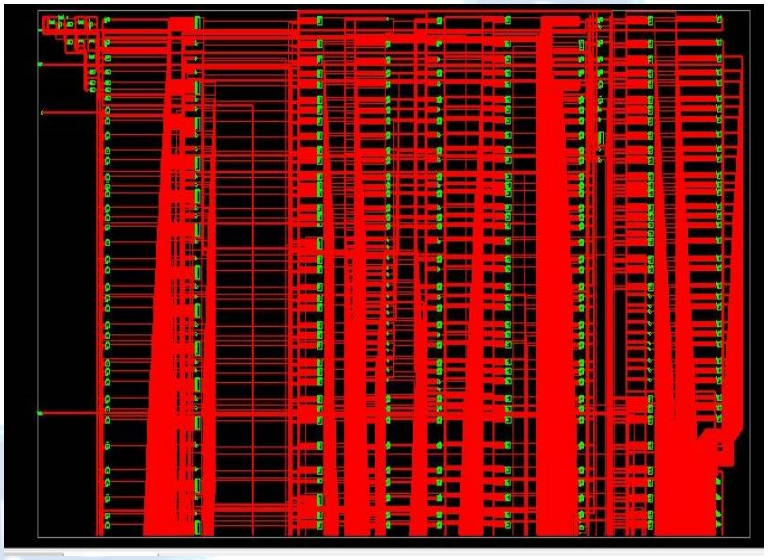

Fig 6: Internal RTL

5.Conclusion:

The aim of work was to enable us to design ICs for the Switching System. Presently switching systems uses

multiplexers, routers, switches etc that leads to low efficiency as they are analog in nature and have a high power requirement. In contrast we have tried to make this whole system digital to increase the efficiency, lower the power requirement, and reduce the delay. VHDL has been used to write all the programs for the ICs because of its user-friendly nature and thus modifications if required for further development shall not prove to be an obstacle. As we know, the process of making ICs is time consuming and an expensive venture so we must be sure about the working results of the ICs in advance as we can't accept errors later.

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