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Design and Analysis of Area Efficient Heterogeneous Fir Filter for DSP Application

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Abstract: The finite impulse response (FIR) is one of the important filters in digital signal processing (DSP) as it responds for finite duration and settles to zero on the finite time. Digital FIR filters are programmable in nature and its behavior can be understood with the help of program and can be easily programmed for the memory of a processor. The digital filters can be replaced without change of the hardware or the external circuitry. The adder is the fundamental building block of the digital circuits such as ALU, microprocessors and microcontrollers, DSP processors and several arithmetic operations. Full adder is the main part of the arithmetic circuits. Full adder circuit is the basic cell of arithmetic circuits.

Keywords: Adder, FIR Filter, Heterogeneous, DSP

1. Introduction:

The signal processing is the field that comprehends the fundamental system level theory, algorithms, implementations and applications of transferring and processing of information from one end to another end. The information may be in the form of several symbols and different physical quantity generally designated as signals. In the real world, both analog and DSP is existing. The analog signal processing is used to design and understand the concept of frequency filters for microprocessors and microcontrollers inputs and outputs. The digital filters are following the digital time signal which is obtained by the sampling of the continuous signals.

The digital filters follow computers and microprocessors to accomplish different mathematical functions and reduce the complexity of actual system. Therefore, the system performance is increased by using digital filters. The filters are used in different types of applications such as Digital Signal Processing (DSP), communication Systems, open and closed loop based digital control systems.The numerical operations and calculations are done by a digital filter fora digital processor over the sampled signal values. The input signal is the analog in nature. It is sampled and digitized with the help ofADCconverter. Such calculation involves the multiplication operation in the input values with some constants and produces the result of that together. In case of the filtered output from the filter, it is needed to convert back the signal into an analog signal using Digital to Analog (DAC) converter. The signal presentation is done using a numbering sequence rather than in the form of current or voltage quantity. The basic steps are shown in Fig. 1.

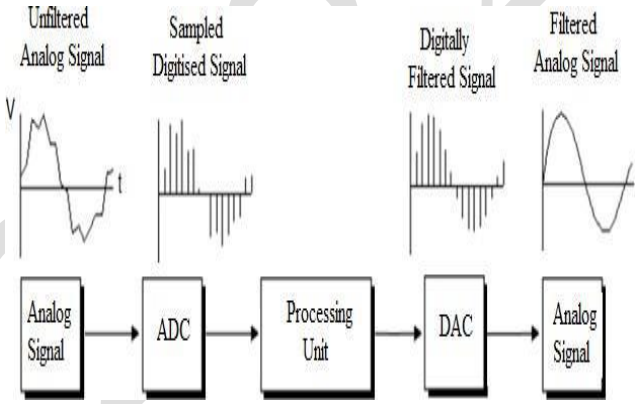

Fig. 1. Digital Filter Processing

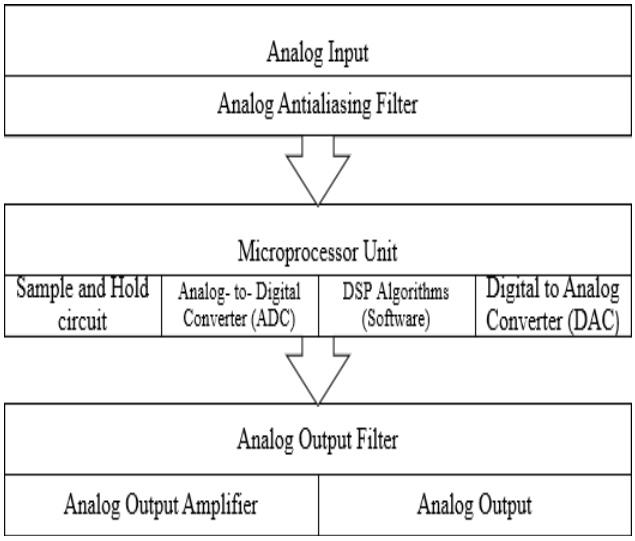

Fig. 2. Digital Filter Units

Fig. 2 depicts the block diagram of the digital filter with its functional unit applicable for any DSP based system. The unfiltered analog input is given to the analog antialiasing filter. The output of this unit is given to the microprocessor unit which understands only digital signals. So, the sample and hold circuit is used to convert the analog signal into sampled outputs and processed by an ADC conversion logic. The ADC output is followed by the microprocessor unit, can be a DSP processor or software-based signal processing for a specific

processor. The output of the processor is digital and given to digital to analog converter and then amplified based on the requirement. The output of the system is a filtered analog signal. The digital processing and filtering inside the DSP processor or microprocessor unit are done with the help of digital circuit-based filters.

2. Literature Review:

Krishna, O. V. (2018)et al[1] research papersuggested the technique for FIR filter realization using Radix-4 adapted Booth multiplication-based architecture and Carry Look Ahead (CLA) adder that can utilize low power. The suggested Booth multiplication logic decreases the increased multiplication period in the complexity of filter weight coefficients and inputs. The CLA is applied to decrease the critical route time of the ordinary ripple carry adder based homogenous adder. They designed the tap -8 filters based on the shortestpath of FIR filter using CLA, and Booth multiplier. The RTL compiler is used in CADENCE tool based on TSMC 180 nm CMOS technology for synthesis process of the FIR filter. The no. of slices, LUTs, IOBs, and DSP elements are 129, 192, 98 and 80. The simulation and synthesis work is done in Xilinx software.

Sharma, P. et al (2015) [5]research papersuggested the method for the realization of the heterogeneous adder. They have used the heterogeneous adder design for FIR filter design. The adder is formed based on 4-bit RCA, 10-bit CLA and 4-bit CSA adders. The designing of each adder circuit is developed using VHDL then 18- bit heterogeneous added is structed. The projected method is applied to improve the delay time of FIR filter realization as an alternativeoption of using direct 16-bit homogenous adder. The designed heterogeneous adder is used to estimate FPGA parameters.

S. AsadAlamet at (2014) [6] research paperproposed FIR filter realization using Logarithmic number system (LNS) methods, used to realize in an easy way because it performs the multiplication in a linear way and addition in a logarithmic way. The coefficients of the FIR filter are placed in its equivalent value of logarithmic. FIR filter the integers are fixed-point values. All the operations are enumerated with discarding the upper and lower bound with their optimization technique. It is also suggested that the selection of three and four bits are the bestsuited solution applied for larger approximated values. The selection of the variables is done that is applicable to suggest the least coverage from the adjacent digit and fits in the right route of the average and branches to maintain minimum distance. The resultant FIR filters are suggested to provide optimal minimax sense under the condition of finite word length. They suggested an approach for the direct realization of finite length word in LNS domain. LNS domain is based on Integer Linear Programming (ILP) in which all the variables have integer values. Further, it is based on branch and bound (BB) algorithm which is based on finding optimized values of integers and combinational.

Qasim S. M. et at (2012) [8]research paperFIR filter of window „N" is used in various DSP use and applications. The output of the filter can be presented by performing linear convolution for filter inputs. The linear structure of the FIR can be program using any HDL and targeted on FPGA. Authors have applied the case of two input sequences x(n) and h(n) of 4 input sequence and the 4 taps filter out is verified on the FPGA. The direct form of the same filter is referred to as a tapped delay line. They suggested the microprogram controller design based on FIR filter operation. It consists of datapath architecture and control unit. Control unit is used to perform various operations relating to the coefficients loading sequentially and their multiplication and processing in the FIR filter. The developed design was designed using VHDL and targeted on SPARTAN-3E FPGA under xc3s500e-4fg320 device in Xilinx 12.2 ISE software. The operational frequency of the design is 119.75 MHz and the designs are capable to perform FIR filter control operations.

3. Methodology:

The working of the heterogeneous Adder FIR filter is shown using Fig. 3. It shows the FIR filter processing for 4 x 4 FIR filter design.

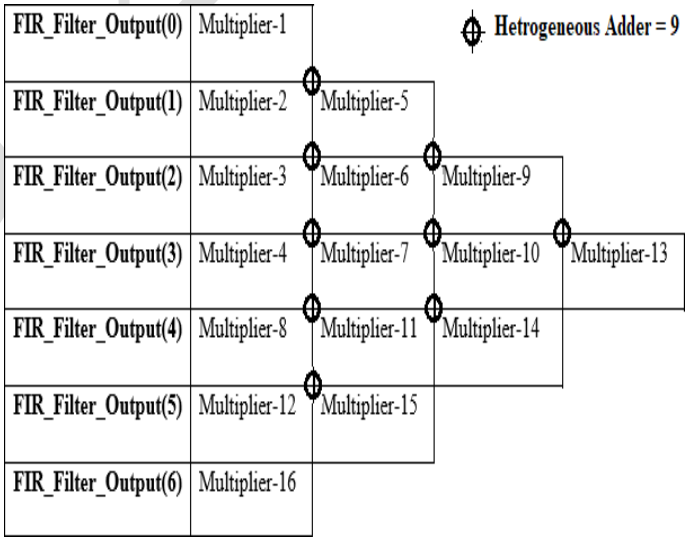

Fig. 3. Heterogeneous FIR filter (4 x 4)

The functionality of the design is easy to understand as the decimal adder-based design in which the coefficients of the FIR filters are directly multiplied with x(n) inputs. The design is following 16 multipliers and instead of decimal adders, we are placing the design using heterogeneous adder. The tree ladder signifies the suggested approach can be good to maintain relationships of delay and space. The decimal adder is following the integer-based design in which the multiplication and addition logic considers 32 bits numbers as the standard input, but heterogeneous adder can process 16 bit or 18-bit data processing based on our requirements and it will take less computation time in multiplication and adding process to save other design on FPGA area and delay.

The FIR filter design and FPGA implementation follow the following steps for the execution. The steps for FIR filter chip implementation are chosen design constraints, apply design approach, follow design modeling, architecture level modeling, RTL analysis, Internal logic schematic in Xilinx software, functional simulation in ModelSim software, apply test cases, FPGA synthesis, parameters analysis, and comparative analysis to estimate the best design approach.

FPGA and Implementation Strategy

The design and complete synthesis process based on FPGA is shown in Fig.5.1. The is methodology is referred as the project flow. The VHDL programming is used to test the all test cases and stimuli inputs. The front-end VLSI design follow all these steps. In the same way all these steps are followed for the DTMF chip design and its real time implementation on FPGA. The EDA tools are used , when the system designed is designing the chip and logic simulation is carried before targeting on FPGA device. The steps description is given as initial design entry, HDL design and modeling, RTL coding, functional gate level simulation, logic synthesis, implementation, generate bit stream, configure SPARTAN 3E FPGA and verify results. In the initial design entry, the designer decides the size of the MIMO system for DTMF and number of input and output subscribers. In the next step of HDL design and modeling, the designer decides the programming language , suitable for the systematic design. The VHDL and Verilog HDL are the main programming languages for the chip design. In the project design flow of MIMO DTMF, the VHDL programming is followed. The modeling of the design is very important. There exist four levels of modeling in VHDL dataflow, behavioral, structural and mixed level of modeling. In the MIMO DTMF the behavioral and structural modeling is followed. The coding is done in keeping the view of RTL with optimal pin number and silicon chip space. The RTL is the schematic view that descripts the input and output of the chip. Then the design is followed by the gate level simulation. The Modelsim software is used to check the functional waveform against inputs and their outputs. After that the logic synthesis is carried out in which the designer, check the hardware resources utilization with respect to the choose FPGA device before the chip design.

The steps and the explanation of the FPGA design concept are shown in Fig. 4. In the design of front end-based VLSI chips, all these steps are followed listed below for all the specific case.

Fig. 7 presents the waveform simulation of CLA (10-bit) chip in ModelSim software. In the waveform, the inputs are a[9-0], b[9-0] and Cin (1-bit) and corresponding output logic are S[9-0] and C[9-0] as the sum and carry outputs. The waveform simulation the test cases are tested as a[9:0] = “1011111110”, b[9:0] = “1111000010”, Cin = „0‟, then S[9:0] = “0000111100” and C[9:0] = “1011000100”. a[9:0] = “0000111100”, b[9:0] = “1111000011”, Cin = „0‟, then S[9:0] = “1111111111” and C[9:0] = “0000000000”.

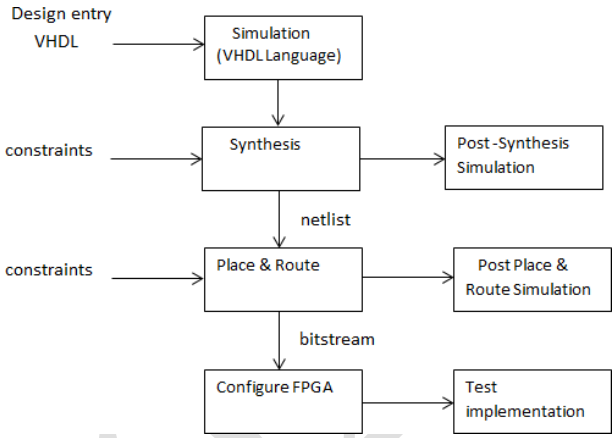

Fig. 4. FPGA Design Flow

4. Result and Discussion:

The Combinational design of heterogeneous adder is having ripple carry adder, carry select adder and look ahead carry adder. The chip design of all individual modules and the integrated chip is presented. The RTL view of 10-bit CLA is shown in Fig. 5 and the internal logic schematic is presented in Fig. 6.

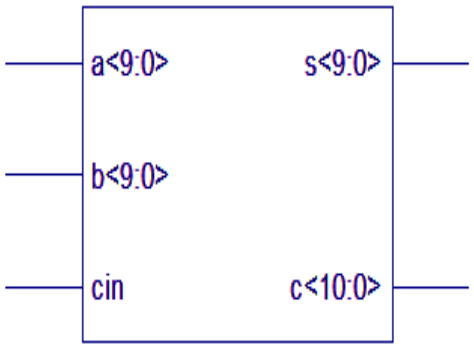

Fig. 5. RTL view of CLA (10- bit)

The Modelsim simulation waveform of the heterogeneous adder-based FIR filter is given in Fig. 8 for binary data inputs and corresponding binary output values. As the heterogeneous adder filter is the combination of RCA, CLA, and CSA. In the last design, the heterogeneous adder is integrated with the FIR filter operation. Instead of using the decimal adder the heterogeneous adder chip is integrated with the functionality of the filter. Rest of the modules of the filter such as multiplication logic is the same. The decimal adder accepts 32-bit input values in VHDL programming hence the multiplication and adder take 32-bit values as in many FIR computations do not need 32-bit operations. The homogeneous adder and heterogeneous adders provide the best alternative way to use the input bit of 16- bit or 18- bit for the adding operations.

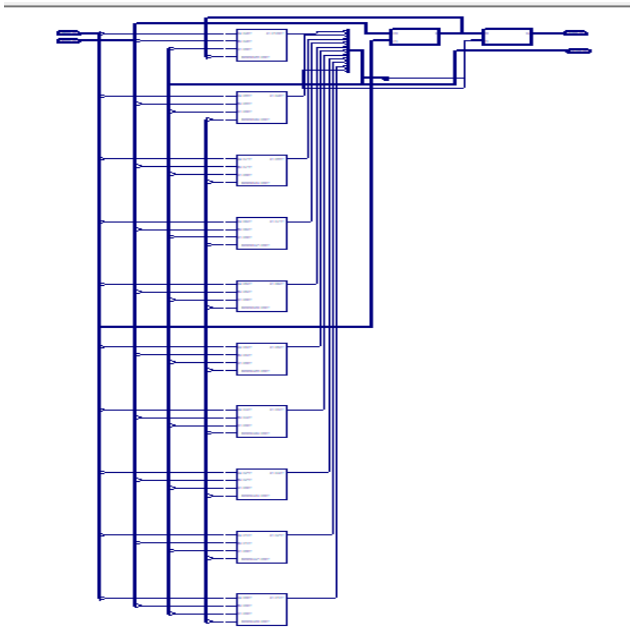

Fig. 6. Internal logic simulation of CLA (10- bit)

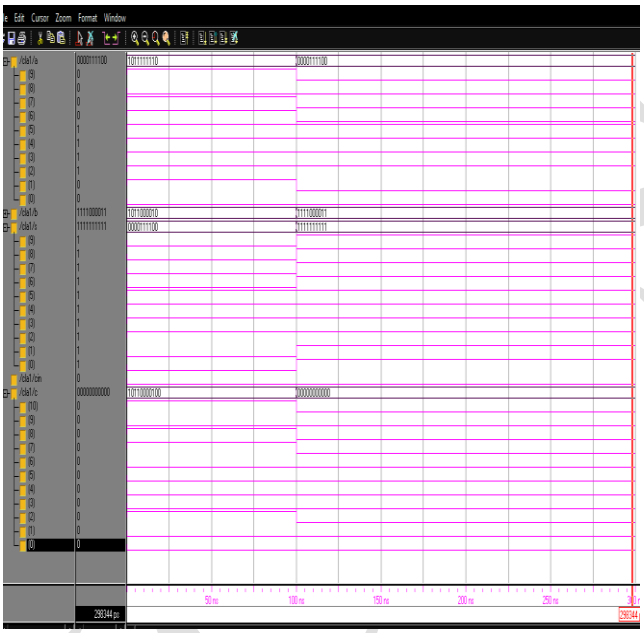

Fig. 7. Waveform simulation of CLA (10- bit) chip in Modelsim

The heterogeneous adder is also having inputs as h0<7-0>, h1<7-0>, h2<7-0>, h3<7- 0> and x_n<7-0>, x_n_1<7-0>, x_n_2<7-0> and x_n_3<7-0> and outputs FIR_filter_output(0)<15:0>, FIR_filter_output(1)<15:0>, FIR_filter_output(2)<15:0>, FIR_filter_output(3)<15:0>, FIR_filter_output(4)<15:0>, FIR_filter_output(5)<15:0>, FIR_filter_output(6)<15:0> for 7 tap operation of FIR filter.

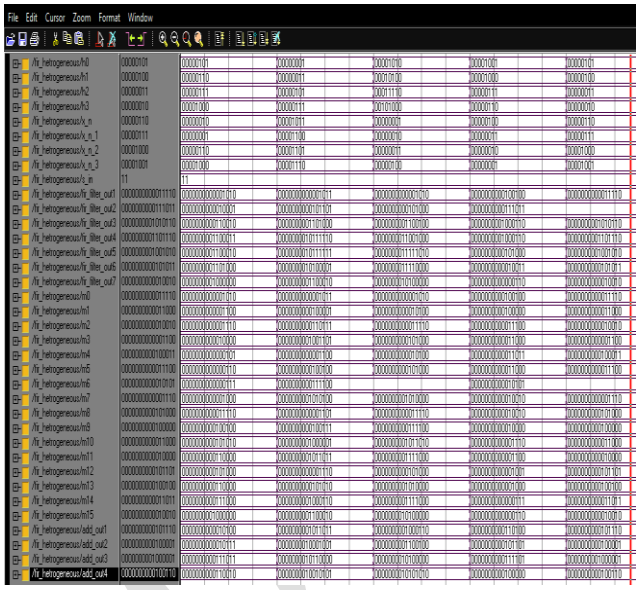

Fig. 8. Heterogeneous adder-based FIR filer simulation in binary

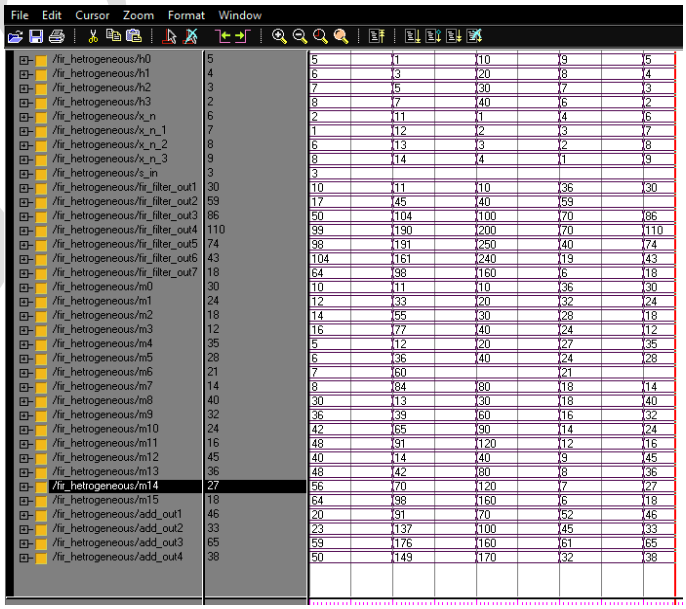

Fig. 9. Heterogeneous adder-based FIR filer simulation in integer (decimal)

5. Conclusion:

DSP systems are following the FIR filters as a basic structure block. The most preference of the FIR filter is that the filters have linear phase and stable properties. The foremost use of the FIR filter is to filter out the undesirable part of the input signal. It provides the shape to the signal after filtering in a communication channel. The chip level implementation of the FIR filter is done using adder module, multiplier module and delay processing elements as the core components. All the components are arranged systematically in the FIR structure based on the structure of the FIR filter. The design of FIR

filter based on decimal adder and heterogeneous adder-based approach is done in Xilinx ISE 14.2 effectively.

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