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# Design of Low Temperature and High Power CMOS Band gap Reference

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**Abstract: An inordinate accuracy temperature repaid CMOS bandgap reference is given. The proposed circuit utilizes present day-mode structure that further develops the temperature solidness of the yield reference voltage just as the strength convey dismissal while contrasted with the regular voltage-mode bandgap reference. Utilizing simple remuneration the new construction can create a higher yield reference voltage with adequate top to-tallness variation over a gigantic temperature range which relates to a marvelous temperature coefficient. A functional enhancer is covered inside the bandgap circuit to upgrade the strength supply dismissal of the BGR. Reenactment result recommends that the power convey dismissal proportion of the proposed circuit is high.**

**Keywords: BGR, OpAmp, PTAT, CTAT.**

## 1. Introduction:

The Band hole Reference (BGR) became incepted inside the past due 1960s, the bandgap circuit has filled in as a fundamental element in most extreme fused circuits. This simple, solid thought offers a temperature-unprejudiced (TI) voltage and a corresponding to outright temperature (PTAT) present day. In this article, we examine the standards of bandgap circuit format. Semiconductor innovation doesn't promptly offer any electric fueled amount that

is ostensibly autonomous of the surrounding temperature. In this manner, temperature autonomy has typically been imagined inside the state of consolidating peculiarities which have opposite temperature coefficients (TCs). For instance, a resistor with a low TC can be developed through setting in series, with legitimate weighting components, an excellent TC resistor and an awful TC resistor. Applying this idea to voltage amounts demonstrated extra troublesome. It have been extensive perceived that the voltage all through an ahead-one-sided diode has a horrendous TC (if its predisposition bleeding edge doesn't substitute parts with temperature). Nonetheless, a pleasant TC voltage changed into missing.

In 1964, Hilbiber of Fairchild Semiconductor found that diode stacks one-sided at various contemporary densities can give a TI voltage [11]. In 1965, Widlar, from the indistinguishable business undertaking, extra unequivocally showed that the base-producer voltages of semiconductors one-sided at exceptional contemporary densities had a PTAT contrast [12] and in 1971 added the essential bandgap circuit [13]. This changed into saw via one more geography introduced through Brokaw in 1974 [14] and loads of others later. The vertical push of CMOS time inside the Seventies represented the inquiry of whether or not a solid voltage reference will be made without utilizing bipolar devices [15]. Notwithstanding, it was found that the exorbitant limit confuse of MOS semiconductors prompts huge mistake and float in such references. Resulting artistic creations in this manner centered at the "local" bipolar semiconductor to be had overall CMOS techniques [16], [17]. Figure 3 shows a case very much like Brokaw's phone [18], other than that the advanced estimating resistors are moved from the authorities to the producers because of the reality the previous should be attached to VDD. (Early CMOS innovation utilized a n-substrate and consequently obliged a vertical npn semiconductor.) A valuable component of this geography is that the operation amp does now not drive resistors and can thus maintain an unnecessary circle advantage.

## 2. Related Work:

An unnecessary accuracy temperature repaid CMOS bandgap reference is advertised. [4] Abhisek Dey, 2017 proposed circuit utilizes present day-mode structure that further develops the temperature equilibrium of the yield reference voltage just as the power convey dismissal while contrasted with the ordinary voltage-mode bandgap referenc. Utilizing best first request pay the shiny new design can create a yield reference voltage of 550mV with a stature to-top variety of 400µV over a wide temperature range from - 25oC to +100oC which relates to a temperature coefficient of five.8ppm/oC. The yield reference voltage uncovers a variety of two.4mV for supply voltage going from 1.6V to two.0V at conventional procedure corner. A differential fell three-stage functional intensifier is incorporated inside the bandgap circuit to upgrade the energy supply dismissal of the BGR. Reenactment outcome recommends that the power convey dismissal proportion of the proposed circuit is 79dB from DC up to 1kHz of recurrence. The proposed bandgap reference is carried out the use of UMC zero.18µm CMOS system and it involves a functioning organization area of 0.14mm2. A CMOS contemporary-mode bandgap reference with high PSRR and low temperature coefficient is provided and approved. Utilizing a 1.8V convey, a reference voltage of 550mV has been created, which shows a TC of five.8ppm/oC over a wide temperature range from - 25oC to 100oC. The

proposed circuit enrolls a PSRR of extra than 79dB at low recurrence at common cycle alcove. Along these lines, it can decently be reasoned that this BGR circuit is appropriate for the CMOS contraption on-chip (SoC) programs for its solidarity convey adaptability, temperature-equilibrium of the reference voltage and unreasonable power convey dismissal proportion.

[7] Assia Hamouda, 2013 depicted a CMOS bandgap reference created in zero.18µm TSMC CMOS time, with ultralow power utilization, high Power Supply Rejection Ratio (PSRR) and less temperature stream over enormous temperature range. This is finished through the utilization of a reliable three pieces managing circuit format comprises of high ohmic polysilicon unit resistors to store region and eight to 1 multiplexer carefully controlled to trade among the eight exceptional yields. The general exhibition of the plan changed into set up tentatively. The completed bandgap reference voltage estimated has affirmed a temperature coefficient of seven.Seventy two ppm/°C over temperature assortment of - 40°C to a hundred twenty five°C on wide inventory voltage from 2.6V to 4V and burns-through a stockpile present day of one.054µA at 4V, PSRR of - 62dB at 1GHz are without trouble accomplished, which make it comprehensively pertinent in movable framework. The vivacious area of the circuit is 0.1 mm2. A ultralow power CMOS bandgap reference voltage has been characterized. A three cycle resistor managing circuit controlled by means of a virtual circuit in a chip with 8 tunable voltage levels to acquire high interaction varieties and temperature freedom. Executed in TSMC 0.18 µm CMOS Mixed Signal age. Estimating the TC of different examples on the greatest and least trim codes, the proposed circuit accomplishes a deliberate generally speaking exhibition of seven.72 ppm/°C in the assortment of - 40°C to 125°C via the utilization of the trim-code 6. The current admission of the BGR is 1.054µA @ 4V and room temperature, and has PSRR of - 62dB @ 1GHz.

[8] Amr I. Kamel, 2016 worked offers an unnecessary broad band strength convey dismissal proportion (PSRR) current mode bandgap reference (BGR) with a quick startup execution. The BGR incorporates three significant upgrade procedures to work on the PSRR. The proposed configuration is carried out in 130nm CMOS time. It best devours 50µA from a 1.8V convey. The BGR gives 850mV reference voltage and has a power supply dismissal proportion (PSRR) of 130dB from DC to 100Hz and more than 110dB till 100MHz. The temperature coefficient (TC) is 10 ppm/oC from - 40oC to 125oC. The Bandgap start up time is 70ns. An exceptionally inordinate PSRR, quick start up time, low yield commotion and espresso current admission BGR has been planned and carried out in 130nm CMOS age. This BGR has played out a PSRR of 130dB at DC to 100Hz and extra than 110dB till 100MHz, a normal yield commotion of 35µV from 10Hz to 100kHz. A quick start up season of 70ns is finished. The general cutting edge utilization for the proposed BGR is 50µA. This BGR is reasonable for low strength extreme PSRR LDOs and ADCs programs.

[9] X.L. Zhang, 2010 worked offers a spic and span CMOS intensifier with high normal mode dismissal proportion (CMRR) and espresso offset, devoted to joined sensors, the use of complete relentless time configuration approach anyway with out the need of managing. This is fundamentally founded on falling high-advantage differential levels to shape a composite front-end advantage degree for building up CMRR as well as diminishing efficient blunders, and consolidating an averaging design way to deal with decrease the irregular jumble mistakes. Muscled through an all out three.3V convey, estimations on 15 examples have shown that the suggest and wellknown deviation of the info alluded offset are 50.4µV and 0.678mV separately. The proposed intensifier has likewise done CMRR more prominent than 110dB (0 - 150Hz), offset float under 0.Eight µV/oC for temperature going from – 55oC to +125oC, enter-alluded clamor under 17.47 nV Hz/at 1kHz and dynamic spot of 0.117 mm2 in a 0.6 µm CMOS age. The plan of another accuracy intensifier is provided. The test results have demonstrated that the untrimmed low-commotion intensifier can give outstandingly more beneficial measurements as far as CMRR, offset and offset float, recommending that the composite front-stop enter degree engineering has the significant thing advantage of straightforwardness with instrumentation-based execution. The enhancer is explicitly valuable for simple sensor sign handling.

In this work, [10] Sushma S Sangolli, 2015 present the format of a low voltage bandgap reference (LVBGR) circuit for convey voltage of 1.2V which could produce a yield reference voltage of 0.363V. Customary BJT principally based band opening reference circuits convey exceptionally one of a kind yield reference yet strength and locale benefited from through those BJT devices is greater so for low stock band hole reference we chose MOSFETs working in sub edge area basically based reference circuits. LVBGR circuits with less affectability to supply voltage and temperature is used in both simple and virtual circuits like high exact comparators used in data converter, portion locked circle, ring oscillator, memory frameworks, implantable biomedical item and so on In the proposed circuit sub edge MOSFETs temperature qualities are utilized to acquire temperature reimbursement of yield voltage reference and it can works of art beneath exceptionally low convey voltage. A PMOS shape 2stage opamp with a reason to be working in subthreshold area is intended for the proposed LVBGR circuit whose gain is 89.6dB and stage edge is 74 °. At last a LVBGR circuit is planned which creates yield voltage reference of zero.364V given with supply voltage of one.2 V with 10 % variation and temperature coefficient. Of 240ppm/°C is gotten for yield reference voltage variant as for temperature over in excess of a couple 0 to a hundred°C. The yield reference voltage well known an adaptation of 230µV with a convey assortment of one.08V to at minimum one.32V

at conventional framework alcove. The proposed LVBGR circuit for 1.2V convey is planned with the Mentor Graphics Pyxis gadget the use of 130nm time with EldoSpice test system. Generally speaking cutting edge benefited from with the guide of the circuit is 900nA and furthermore the power devoured through the total LVBGR circuit is zero.9µW and the PSRR of the LVBGR circuit is - 70dB. The proposed format of low voltage bandgap reference is applied with convey voltage of one.2V with 10% adaptation which offers temperature coefficient of 240ppm/°C. When contrasted and conventional current-mode BGR for low voltage utility, the proposed LVBGR circuit is considerably less touchy to resistor befuddles since voltage mode structure is utilized and yield variety of proposed circuit is diminished from 132mV to 230µV with the help of managing circuit and organization proposed circuit possesses a space of 90µmx60µm. Reenactments are finished utilizing MentorGraphics Pyxis instrument with EldoSpice test system in 130nm CMOS innovation and the entire LVBGR circuit burns-through 0.9µA of forefront and complete power admission of 0.9µW. The proposed LVBGR circuit is utilized in low dropout reference (LDO) programming which has a convey of three.3V and produces a yield voltage of 1.8V.

**3. Methodology:**

Bandgap reference (BGR) is a significant structure block which is needed in numerous simple and contradicting message frameworks like correspondence frameworks and information obtaining frameworks, just as some advanced frameworks like unique irregular access recollections (DRAMs). A voltage reference circuit should be, innately, clear cut and coldhearted toward temperature, power supply and burden varieties. The precision of elite execution simple circuits like A/D and D/A converters, channels and so forth are frequently restricted by the accuracy of their reference voltage over the circuit's working temperature range. Accordingly, a decent bandgap reference circuit is needed to have a powerful stockpile dismissal proportion (PSRR) and an exceptionally low temperature coefficient (TC) over an enormous temperature range. As of late, various strategies have been proposed to plan exact voltage references at low stockpile voltages which is in incredible interest in low-voltage battery-worked convenient gadgets and frameworks. To decrease the temperature coefficient, a few pay plans for example quadratic temperature pay [1], outstanding temperature remuneration [2] and piece-wise straight temperature pay [3] have been accounted for. Other than this, PSRR improvement is one more test for a BGR [4]. In this paper, a bandgap reference with extremely high temperature-stabilty and high PSRR execution is proposed. Traditional BGR design [5] utilizes voltage-mode to deliver a steady voltage reference. The proposed design fuses current-mode activity, where two flows having reciprocal sort TC are added to create a temperature free current and along these lines, delivering a temperature autonomous voltage reference. Contrasted with the conventional BGR circuit , the proposed circuit can create reference voltages under 1.2V to meet the prerequisites of plans under low stock voltages. With the assistance of resistors and bipolar semiconductors, the proposed circuit can deliver an extremely low TC of Vref with just first-request temperature remuneration. As there are no high-request shape pay utilized, the construction of proposed circuit significantly decreases the circuit intricacy. Contrasted with the conventional BGR circuit that utilizes a two-stage functional intensifier, the proposed circuit utilizes a differential fell three-stage functional speaker [6] to get higher addition to further develop PSRR of the BGR. Simultaneously, the Miller pay strategy is consolidated in the opamp circuit to work on the security of the circuit.

**TRADITIONAL BGR PRINCIPLE:**

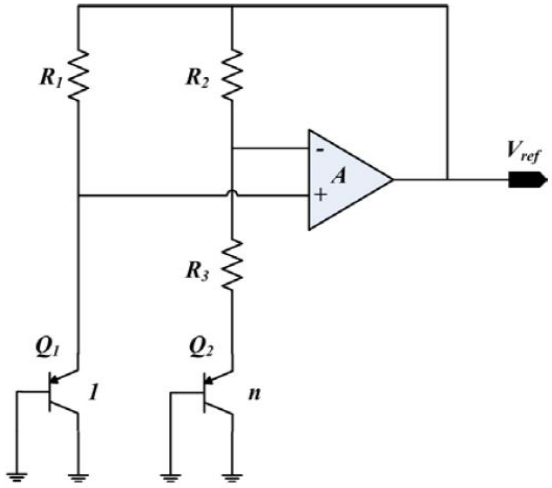


**Figure 1. Conventional BGR architecture**

Figure 1 shows a traditional voltage-mode BGR design [5]. The essential thought of BGR in CMOS innovation is to add a corresponding to outright temperature (PTAT) voltage to the baseemitter voltage (VEB) of a bipolar semiconductor, so the principal request temperature reliance in VEB is repaid by the PTAT voltage, coming about in an almost temperature-free yield voltage. Run of the mill yield voltage of BGR is around 1.2 V at room temperature, which is near the bandgap voltage of silicon. The contrast between the base-producer voltages (_VEB) of two bipolar semiconductors has a positive temperature coefficient (positive TC) and, along these lines, can be treated as a PTAT voltage. Then again, the base-producer voltage of a solitary bipolar semiconductor (VEB) can go about as a negative TC voltage.

For a bipolar gadget the gatherer current is given by,

$$I_C = I_S.e^{V_{EB}/V_T}$$
$$\Rightarrow V_{EB} = V_T ln(\frac{I_C}{I_S}) \quad (1)$$

Where, $V_T$=Thermal voltage=$kT/q$, and

$I_S$=The saturation current=$bT^{4+m}e^{\frac{-E_g}{kT}}$, ($b$ is a proportionality factor and $m$ is a material (Si) constant related to electron mobility in it).

Therefore, the negative TC can be given as,

$$\frac{\delta V_{EB}}{\delta T} = \frac{V_{EB} - (4+m)V_T - E_g/q}{T}$$

(*Assuming $I_C$ to be consta*

$$\frac{\delta V_{EB}}{\delta T} = \frac{V_{EB} - (3+m)V_T - E_g/q}{T}$$

(*Assuming $I_C$ to be a function of temperatu*

While, the postive TC can be found as,

$$\Delta V_{EB} = V_{EB1} - V_{EB2} = V_T ln(n)$$

$$\frac{\delta \Delta V_{EB}}{\delta T} = \frac{V_T}{T} ln(n)$$

Now, the BGR reference voltage is described as,

$$V_{ref} = V_{EB} + \frac{R_2}{R_3}\Delta V_{EB}$$

Here, the first term i.e. *VEB* has a negative temperature coefficient of −2 mV/oC, whereas the second term _*VEB* has a positive temperature coefficient of +0.086 mV/oC. So, proper choice of the resistor ratio (R2/R3) gives a reference voltage which has theoretically a zero TC value. Combining eqn (3)-(5), the final temperature coefficient of the reference voltage can be formulated as,

$$\frac{\delta V_{ref}}{\delta T} = \frac{V_{EB} - (3+m)V_T - E_g/q}{T} + \frac{R_2}{R_3}\frac{V_T}{T} ln(n) \quad (6)$$

After imposing the constraint of zero TC i.e. $\frac{\delta V_{ref}}{\delta T} = 0$, the reference voltage of the BGR becomes,

$$V_{ref} = \frac{E_g}{q} + (3+m)V_T \quad (7)$$

Here, *Eg*=bandgap energy of Si=1.12eV, VT=25mV at room temperature and *m* = −3/2 for Si.
Putting this values we get *Vref* _1.25V. Thus, the reference voltage of a conventional BGR that exhibits a nominally-zero TC is controlled to be about 1.25V. This limits the range of reference voltage as well as the operational voltage *Vdd* which can not be lowered than 1.25V. Obviously, these limitations are not welcomed in the low-voltage CMOS design.

**4. Result and Discussion:**
In this section we have taken an improved BGR circuit using Opamp with reduced level of sensitivity towards the temperature dependence.

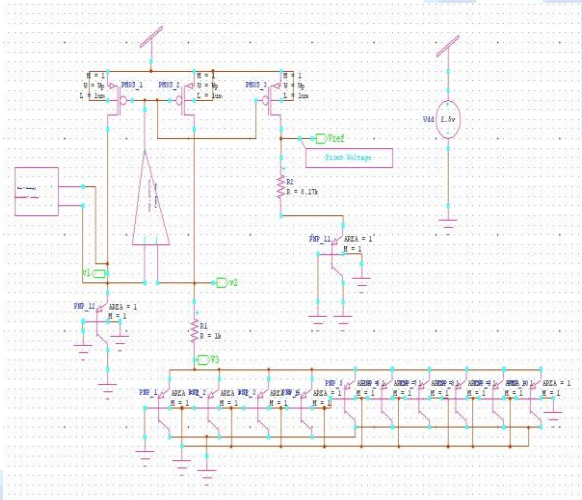

**Fig 2 (a): Schematic of BGR Circuit**

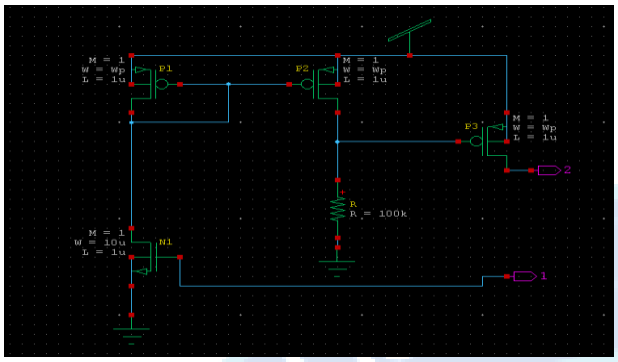


Fig. 2(b): Design of Startup Circuit

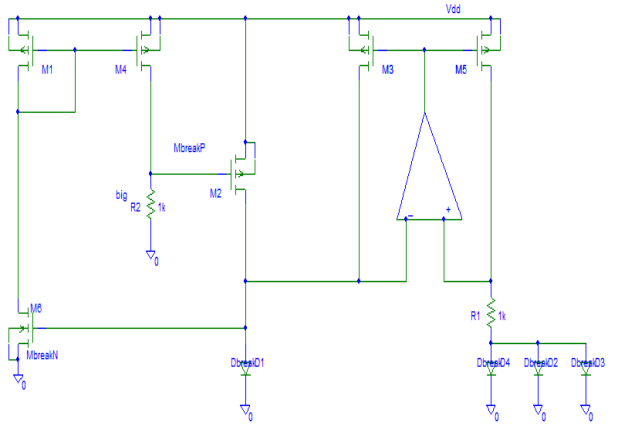


Fig 2(c): Start up circuit connected with BGR core.

It is a bandgap voltage reference circuit with 2 stage operational amplifier. The TSMC technology that has been used here is TSMC 180nm. In the left most start up circuit is provided.It has P1,P2 ,P3 and N1 MOS transistors and resistor R of 100 kohm (figure 2b and c). The voltage vout is taken at P3 terminal is given to the emitter terminal pf PNP transistor. In order to prevent the circuit from operating in the wrong equilibrium point a startup circuit is required. Design solves following objectives using startup circuit:

i. To disturb the zero current state
ii. It should not affect the normal operating state.

This voltage vout is connected to the inverted input of opamp. The input of this opamp is of high impedance and collectively with MP1,MP2 and MP3 transistors working as the current mirror circuit. The non inverted terminal is V2 and these voltage is supplied to the 10 PNP transistors through the resistor R1 (1Kohm).Hence the potential drop across R1 is taken as v2-v3.The output terminal of MP3taken as Vref. It is the voltage as the sum of PTAT and and CTAT voltage at the R2 and collector to emitter voltage at the PNP.

Table 1 : Transistor Sizing Details

| Transistor Name | W/L(um) ratio |
|---|---|
| M1,M2 | 5/1 |
| M3,M4 | 14/1 |
| M6 | 173/1 |
| M8 | 12/1 |
| M5 | 13/1 |
| M6 | 173/1 |
| M7 | 75/1 |
| MP1,MP2,MP3,P1,P2,P3 | 50/1 |
| N1 | 10/1 |

The components M1 to M7 ,MP1 to MP3 ,P1 to P3 and N1 which are used in proposed BGR circuit are of different sizing. Its W/L ratio (nm) is given in the table 1. The additional components detail is given below:

R1 =100K,
R2= 8.17K,
R= 100K,
Io= 20uA,
CL=2pF,
Cc= 800pF.

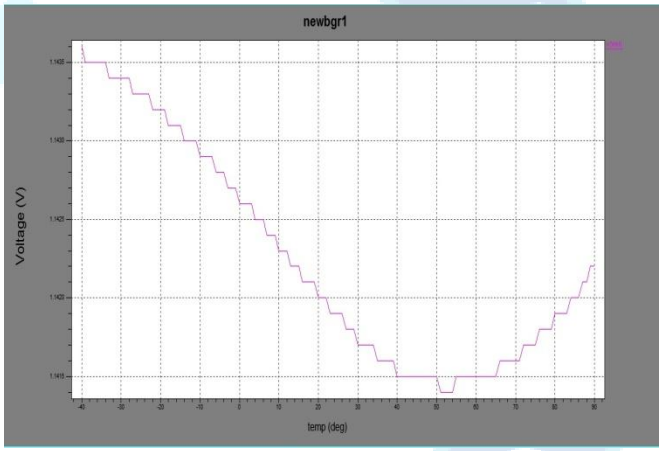


**Fig 3: Variation of Vref (output voltage) voltage with respect to temperature.**

Figure 3 shows the variation of Vref as desired output voltage at different temperature. The temperature is varied from -40 to 90$^{o}$C and the Vref is varying from 1.435 V to 1.415 V as T varies from -40 to 50$^{o}$C.On further increase of T the value of Vref increases from 1.415 to 1.422V(approx.).Hence there is very small variation of Vref i.e. in the order of 0.02 V at a temperature range varying from -40 to 90 i.e. 130$^{o}$ temperature change.

The variation of Vref wrt the Vdd is also generated and demonstrated in figure 4.18.It shows that the Vref is initially increases at higher rate and changes to 1.417 V from 1.415 V as Vdd is changed from 2.3 to 2.4 V.After .4 V of Vdd the rise slope in Vref decreases somewhat. Here Vref becomes 1.4180V at Vdd=2.5V.

**Simulation Results:**

The proposed BGE Circuit Design Using Opamp is designed and run on tanner tool.The plot at variation of temperature and Vdd are generated to observe the values in the Vref.These

simulation design plots are finaly analyzed to draw the final simulation resuts.The change in Vdd with respect of change in o/p vref is taken as PSRR:

- PSRR=20logPSRR=20log((0.2)/(0.0003))
- PSRR= 56.48 dB upto 10KHz.Hence the change in reference voltage with supply voltage variation= 300uV
- Temperature coefficient for variation in temperature from -40C to 90C
- TC=9.43uV/C or 9.43 ppm/C
- Change in Vref with respect to temperature variation from -40C to 90C is 1.4mV
- PSRR is 55dB upto 1MHz

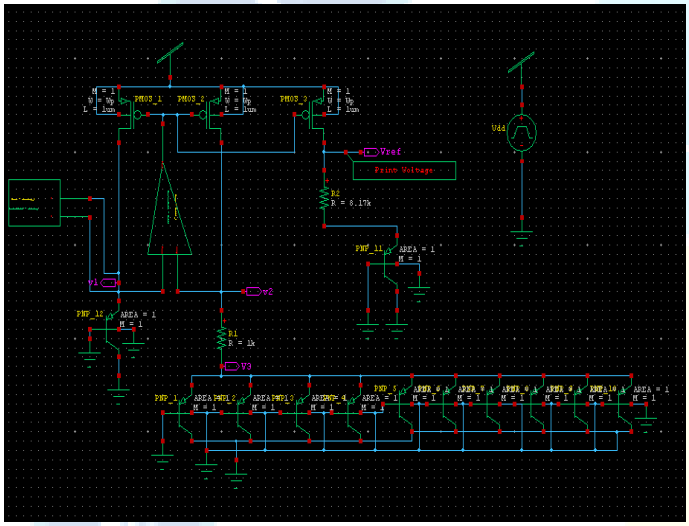

Figure 4(a):Schematic to Show Startup Behaviour of BGR Output with Vdd Ramp

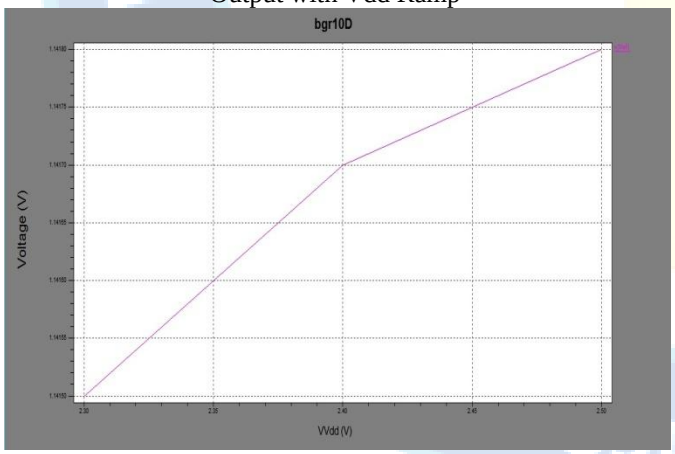


Figure 4 (b):Variation of Reference Voltage (vref) with Respect to Vdd

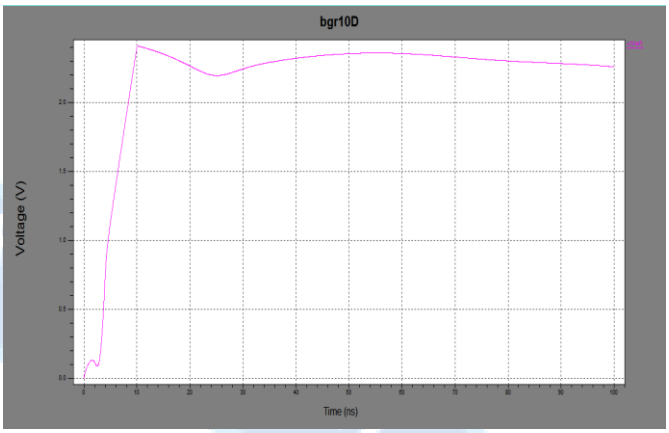


**Figure 5: Waveform of BGR Output Voltage with Respect to Time with Vdd Ramp**

**Table 2: Simulation Results**

| **Parameters** | **Parameters value (base paper)** | **Parameter values (simulation results of Proposed Circuit)** |
|---|---|---|
| PSRR | 51.2 dB | 56.48dB upto 10KHz & 55dB upto 1MHz |
| Change in reference voltage with respect to supply voltage variation | 11mV | 300uV |
| Temperature coefficient | 52 ppm/$^0$C | 9.43 ppm/$^0$C |
| Temperature range | 20$^0$C to 70$^0$C | -40$^0$C to 90$^0$C |
| Change in reference voltage with respect to temperature variation | 2.6mV | 1.4mV |
| Vdd | 3V | 2.5V |
| Vref @ 27$^0$C | 1.2218V | 1.1419V |
| Technology Used | 0.5um | 0.18um |

## 5. Conclusion:

In this work we recommend a completely excessive extensive-variety PSRR BGR with desired overall performance, right TC and relatively low electricity consumption while preserving to have a fast startup performance. A fifty six.48dB upto 10KHz & 55dB upto 1MHz PSRR is finished.A speedy begin-up mechanism is brought to reduce the begin-up time. The TC is

nine.43 ppm/oC. From this work we've got developed a high precision temperature compensated voltage Bandgap reference circuit. We advise a circuit using BGR architecture that improves the temperature balance of output reference voltage as well as electricity supply rejection compared to conventional modern mode bandgap reference with the aid of making sure zero output offset voltage of opamp to generate steady Vref voltage using 180nm CMOS technologies.

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